REMARKS

Claims 1, 3-4, 52-54, and 66-85 are pending in the present application. Claims 52, 70-72, and 85 have been rejected under § 112 as being indefinite. All of the pending claims have been rejected under § 103 as being unpatentable over Bradley, US 6,087,865 (Bradley) in view of Dufour, US 6,111,470 (Dufour).

Information Disclosure Statement

An IDS is being submitted electronically on 4/13/04 to cite US Patent 5,880,024. Applicant's request consideration of the reference cited in the IDS.

Section 112 Rejections

The examiner states that, in claim 52, it is unclear how the recitation "VCO and PLL circuitry is misdescriptive. Claim 52 has been amended in response to the Examiner's concerns. The amendments to claim 52 were not made to distinguish the prior art. In a previous Office Action, the Examiner rejected claim 52 stating that it was not understood what the "techniques" are and how they can be applied. The Specification of the present invention teaches several techniques that can be used alone, or in combination with others, to reduce interference. Claim 52 includes applying one or more techniques to reduce interference near the frequency of an output of the VCO circuitry. While the Specification provides several specific examples of how interference can be reduced, claim 52 generally recites the application of one or more techniques to reduce the interference.

The examiner states that, in claims 70-72, 81-82, and 85, it is not understood what the "clock rate" is, how the divider can be clocked at the rate, and how this limitation is read on the preferred embodiment or seen in the drawings. In these claims, the term "rate" has been replaced with "frequency". These amendments to claims 70-72, 81-82, and 85 were not made to

distinguish the prior art. Applicants submit that a person of ordinary skill in the art reading the claims in light of the Specification would understand the scope of the claims. Applicants believe that the claims are supported by the Specification. The Specification discusses reducing digital current in dividers to reduce interference. For example, referring to FIG. 4, the Specification states that,

> "Figure 4 shows a first divide-by-R1 counter 204 and a second divide-by-R2 counter 205. To divide by 65, R1 is given a value of 5 and R2 is given a value of 13, resulting in a total division of 65. This arrangement results in less digital current since the components of the counter 205 are clocked at f_{REF}/R1 rather than at f_{REF}. In addition, less support logic is required in a fixed counter versus a universally programmable counter. (Spec., page 15, lines 6-11).

The examiner states that, in claim 85, it is not understood what the "need" on line 3 and "components" on line 4 are, and how the need can be identified, and how the components can be minimized. Claim 85 has been amended to claim a "method of reducing interference in a circuit formed on an integrated circuit, the circuit having one or more dividers," including "selecting a divider in the circuit". Claim 85 has been further amended to recite "wherein each of the plurality of fixed-value dividers is configured to divide by a respective fixed non-programmable division factor." Claim 85 was also amended to replaced "required" with "used" in line 4. Applicants argue that the meaning of "selecting a divider" from a "circuit having one or more dividers" is clear. With respect to "minimizing the number of circuit components used by the selected divider", applicants also submit that this language is clear. One example of minimizing the number of circuit components used by a divider is to replace a programmable counter with a fixed-value divider. For example, the Specification states that,

> "The present invention reduces the digital current by reducing the number of components in the divide-by-R counter. This is accomplished by replacing the programmable counter by one or more fixed-value counters and clocking at least one of the counters at a slower rate." (Spec., lines 21-24).

Prior Art Rejections

All of the pending claims have been rejected under § 103 as being unpatentable over Bradley in view of Dufour. The examiner argues that it would have been obvious to implement the PLL circuit of Bradley on an integrated circuit as taught by Dufour, for the purpose of reducing size. The examiner states that Bradley discloses a PLL circuit 203, comprising a first divider 221 and a second divider 220 (Figure 5).

Amended claim 1 claims a method of reducing interference in a circuit having a PLL, including "providing a divider circuit at the input of the PLL for dividing the frequency of an input signal by a desired amount" and "wherein the divider circuit is provided by placing first and second fixed-value dividers connected in series at the input of the PLL, wherein the first and second fixed-value dividers are configured to divide by respective first and second fixed non-programmable division factors."

In contrast, the prior art cited by the examiner uses programmable dividers. In the Bradley patent (entitled "Programmable Frequency Divider"), the field of the invention states that "the present invention relates to a programmable frequency divider utilizing components to eliminate undesirable output harmonics while reducing overall required circuitry and power consumption." (Col. 1, lines 13-16). Also, in the Office Action, the Examiner points out on page 3 that "the dividers in the Bradley reference can be selectable." Further, when describing the frequency synthesizer of Figure 5, including the divide by R divider 220 and the divide by Q divider 221, Bradley states,

> "A user may select values for Q, R, and M so that equations 17 and 18 are satisfied for the user's desired value of N. The value for M may be altered depending on the selected value for F_S. As with the circuit shown in FIG. 4, values of Q, R and M may be selected so that oscillators operating over the same frequency range may be used for the signal generator 200 as well as the VCO 210. (emphases added) (Col. 7, lines 18-23).

Bradley does not teach or suggest the use of fixed-value or non-programmable dividers as the claims recite. For at least these reasons, it is believed that amended claim 1 is allowable over the prior art. Since claims 3 and 4 depend from amended claim 1, it is also believed that these claims are allowable.

Amended claim 66 claims a method of reducing interference in a circuit including "providing a first fixed-value divider having an input and an output, wherein the first fixed-value divider is configured to divide by a first fixed non-programmable division factor" and "providing a second fixed-value divider having an input and an output, wherein the second fixed-value divider is configured to divide by a second fixed non-programmable division factor." For at least the reasons set forth above with respect to amended claim 1, it is believed that amended claim 66 is also patentable over the prior art. Since claims 67-76 depend from amended claim 66, it is also believed that these claims are allowable. Note that in line 2 of claim 66, "and requiring" has been replaced with "that includes". This amendment on line 2 of claim 66 was made to make the claim more clear, not to distinguish prior art.

Amended claim 77 claims a circuit for reducing interference on an integrated circuit including "a divider formed on the integrated circuit ... wherein the divider further comprises: a first fixed-value non-programmable divider for receiving an input signal and dividing the input signal by a first fixed amount, and a second fixed-value non-programmable divider for receiving the divided signal from the first fixed-value divider and further dividing the input signal by a second fixed amount." For at least the reasons set forth above with respect to amended claim 1, it is believed that amended claim 77 is also patentable over the prior art. Since claims 78-79 and 81-84 depend from amended claim 77, it is also believed that these claims are allowable.

Amended claim 85 claims a method of reducing interference in a circuit formed on an integrated circuit including "selecting a divider in the circuit", "minimizing the number of circuit components used by the selected divider by using a plurality of fixed-value dividers rather than one or more programmable dividers, wherein each of the plurality of fixed-value dividers is configured to divide by a respective fixed non-programmable division factor" and "clocking at least one of the plurality of fixed-value dividers at a lower frequency than other fixed-value dividers in the circuit." For at least the reasons set forth above with respect to amended claim 1, it is believed that amended claim 85 is also patentable over the prior art.

Amended claim 52 claims a method of integrating PLL circuitry for a wireless communication system onto a single integrated circuit including "forming the integrated circuit having PLL circuitry integrated on the integrated circuit, the PLL circuitry including VCO circuitry" and "applying one or more techniques to reduce interference present near the frequency of an output signal of the VCO circuitry." Neither reference cited by the Examiner appears to teach techniques for reducing interference present near the frequency of an output of VCO circuitry, as recited by amended claim 52. It is therefore believed that amended claim 52 is also patentable over the prior art. Since claims 53-54 depend from amended claim 52, it is also believed that these claims are allowable.

Conclusion

It is respectfully submitted that all claims are patentable over the prior art. It is further more respectfully submitted that all other matters have been addressed and remedied and that the

application is in form for allowance. Should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Bruce A. Johnson, Applicants' Attorney at 512-301-9900 so that such issues may be resolved as expeditiously as possible.

Respectfully Submitted,

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